AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF THE CLAIMS:

1. (currently amended) A semiconductor device comprising:

a memory chip including first bonding pads ~~which are~~for address arranged along a first side of the memory chip, ~~corresponding to address terminals~~ and second bonding pads ~~which are~~ for data arranged along a second side which faces the first side in an opposed manner ~~corresponding to data terminals~~;

a package substrate including first bonding leads ~~which are formed~~ arranged along a first side of the package substrate corresponding to the first side of the memory chip, and second bonding leads ~~which are formed~~ arranged along a second side of the package substrate corresponding to the second side of the memory chip~~, and address terminals and data terminals which are connected to the bonding leads~~;

a semiconductor chip ~~which includes~~ including third bonding pads arranged along a first side thereof, an address output circuit, fourth bonding pads arranged along a second side thereof which faces the third side in an opposed

manner, ~~and~~ a data input/output circuit which ~~are also~~ serves ~~served~~ for memory access, and a signal processing circuit having a data processing function,

wherein the first and third bonding pads ~~which~~ are connected in common to the first bonding leads of the package substrate ~~corresponding to the address terminals~~ and the second and fourth bonding pads ~~which~~ are connected in common to the second bonding leads of the package substrate ~~corresponding to the data terminals are arranged so as to be distributed to two sides out of four sides~~, and

wherein the memory chip and the semiconductor chip are mounted on the package substrate in a stacked structure.

2. (currently amended) A semiconductor device according to claim 1, wherein wires are used to connect said first and third bonding pads to said first bonding leads and to connect said second and fourth bonding pads to said second bonding leads~~the corresponding terminals of the semiconductor chip and the memory chip are connected to each other by wires with respect to the bonding leads which are formed in common on the package substrate~~.

3. (currently amended)A semiconductor device according to claim 1,

wherein ~~in conformity with pitches of respective~~ the first and second bonding pads are arranged with a correspondence to pitches of the third and fourth bonding pads, respectively~~of address and data of the memory chip, the respective bonding pads of the corresponding address and data of the semiconductor chip are arranged~~, and

wherein ~~between the respective bonding pads for address and data of the semiconductor chip,~~ fifth and sixth bonding pads ~~which~~ are independently formed along opposing sides of ~~on~~ the semiconductor chip between said first and second bonding pads~~so as to conform to the memory chip side pitch are suitably arranged~~.

4. (currently amended)A semiconductor device according to claim 1, wherein the package substrate includes ~~forms~~ first wiring layers ~~respectively~~ on a front surface thereof on which the memory ~~semiconductor~~ chip is mounted, and second wiring layers on a back surface thereof on which balls constituting external terminals are formed, and the first wiring layers are connected to corresponding second wiring layers ~~are connected~~ via through-holes ~~by through holes~~.

5. (currently amended)A semiconductor device according to claim 4,

wherein the semiconductor chip constitutes a one chip microcomputer, and

wherein bonding pads on third and fourth sides of the semiconductor chip ~~which are connected~~ are electrically connected to respective ones of said external terminals ~~necessary for the microcomputer are also arranged on remaining two sides out of four sides~~.

6. (currently amended) A semiconductor device according to claim 5,

wherein the memory chip has an area larger than an area of the semiconductor chip and is formed into a rectangular shape in which a length of the first side and the second side is shorter than a length of ~~other~~ two other sides, and

wherein ~~with respect to rows of the bonding leads which are formed corresponding to the first side and the second side of the memory chip, the pull out~~ directions of wires of the first wiring layers leading from said first and second bonding leads to the ~~through holes~~ through-holes are arranged to extend toward an inner region of ~~the inside of~~ the package substrate.

7. (currently amended) A semiconductor device according to claim 6,

~~wherein the memory chip is mounted on the surface of the package substrate, and~~

wherein the semiconductor chip is mounted on a surface of the memory chip so as to provide a stacked structure.

8. (currently amended) A semiconductor device according to claim 5, wherein ~~with respect to the rows of bonding leads which are formed corresponding to two sides other than the first side and second side of the memory chip, the pull-out~~ the package substrate has third and fourth bonding leads arranged respectively along third and fourth sides of the package substrate, and directions of wires of the first wiring layers leading from the third bonding leads to ~~the through holes~~ through-holes are distributed toward the inner region and an outer region ~~the inside and the outside~~ of the package substrate relative to the third bonding leads, and directions of wires of the first wiring layers leading from the fourth bonding leads to through-holes are distributed toward the inner region and the outer region of the package substrate relative to the fourth bonding leads.

9. (currently amended) A semiconductor device according to claim 8, wherein ~~with respect to a length of~~

~~the bonding leads which are formed corresponding to the first side and the second side of the memory chip, a length of the bonding leads which are formed corresponding to two sides other than the first side and the second side of the memory chip is made~~ said third and fourth bonding leads are shorter in length than said first and second bonding leads.

10. (currently amended) A semiconductor device according to claim 6, wherein at least some of the first bonding leads and the second bonding leads ~~of the package substrate corresponding to the first side and the second side of the memory chip~~ are formed into ~~a~~ rectangular configuration ~~shape~~ such that ~~the~~ longitudinal directions of those first bonding leads are substantially aligned with extension directions of wires which connect those first bonding leads with corresponding first and third bonding pads, and longitudinal directions of those second bonding leads are substantially aligned with ~~thereof is directed in the~~ extension directions of wires which ~~perform the connection of the~~ connect those second bonding leads with ~~the~~corresponding second and fourth bonding pads ~~of the corresponding memory chip and the semiconductor chip corresponding to the bonding leads~~.

11. (withdrawn, currently amended) A semiconductor device according to claim 7, wherein ~~the~~ said first and second bonding leads ~~which are respectively formed corresponding to the first side and the second side of the memory chip are~~ include bonding leads having notched portions ~~thereof~~ over which wires connected to other bonding leads pass ~~notched~~.

12. (withdrawn, currently amended) A semiconductor device according to claim 10,

wherein ~~the~~ said first and second bonding leads ~~which are respectively formed corresponding to the first side and the second side of the memory chip~~ are arranged in a staggered manner, each in two inner and outer rows along ~~the~~ extension directions of wires which are connected thereto ~~the bonding leads~~, and

wherein notched portions are formed ~~on~~ at inner ends of ~~the inside~~ bonding leads in said inner rows.

13. (withdrawn) A semiconductor device comprising:

a semiconductor chip which includes bonding pads arranged along at least a first side and a second side which faces the first side in an opposed manner; and

a package substrate which includes bonding leads formed corresponding to the first side and the second side

of the semiconductor chip and external terminals connected to the bonding leads,

wherein the bonding leads have portions thereof over which wires connected to other bonding leads pass notched.

14. (withdrawn) A semiconductor device comprising:

a semiconductor chip including bonding pads which are arranged along at least a first side and a second side which faces the first side in an opposed manner; and

a package substrate including bonding leads which are formed corresponding to the first side and the second side of the semiconductor chip and external terminals which are connected to the bonding leads,

wherein the bonding leads are arranged in a staggered manner at two inner and outer rows along the extension direction of wires which are connected to the bonding leads,

wherein the pull-out direction of wiring layers leading to respective lead through-holes are directed toward the inside of the package substrate, and

wherein notched portions are formed in inner ends of the inside bonding leads at the two inner rows.